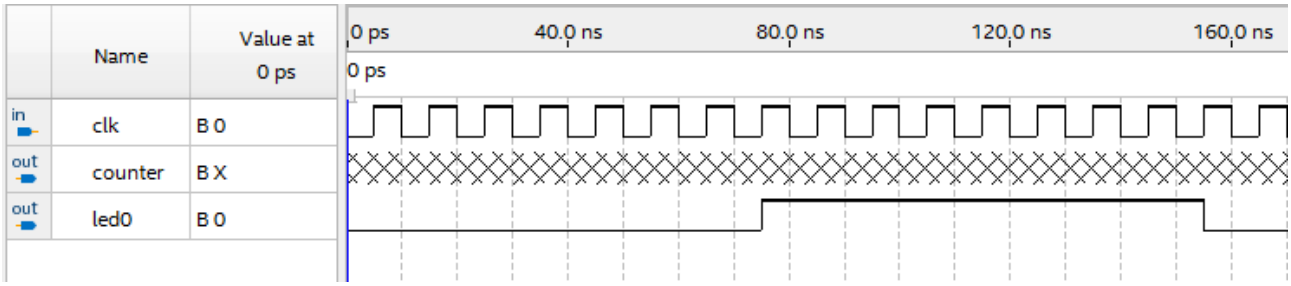
Делитель синала / частоты на 8




```
module freg_div8
(
output led0,
input clk,
output reg counter = 1'b0
);

assign led0 = counter;
reg[2:0] count8;

always @(posedge clk)
begin
        count8=count8+1;
        if (count8==0) counter = !counter;
end
endmodule
```